WHAT IS CLAIMED IS:

1. A device for fault testing in a microprocessor chip comprising:

a test unit having a first reference signature representing faults at a first frequency;

a loading unit for receiving and outputting masking data; and

a masking unit coupled to the loading unit, the masking unit generating a second reference signature based on the masking data and scanning data from a scan string in the chip, wherein the second reference signature replaces the first reference signature such that the test unit represents faults at a second frequency.

2. The device for fault testing of claim 1 further comprising a file unit connected between the output of the loading unit and the input of the masking unit, the file unit feeds back the masking data to the loading unit for saving a reloading time after the testing.

3. The device for fault testing of claim 2, wherein the file unit further comprises multiple latches, wherein the number of latches of the file unit is equal to or greater than latches in the scan string on the chip.

4. The device for fault testing of claim 2, wherein the file unit includes a scan-only register.

5. The device for fault testing of claim 2, wherein the file unit performs an exclusive testing to a predetermined latch.

6. The device for fault testing of claim 5, wherein the latches of the file unit shift bit-by-bit and match with latches in the scan string, respectively, corresponding to a clock.

7. The device for fault testing of claim 1 further comprising a control unit connected between the output of the file unit and the input of the masking unit, wherein the control unit controls the file unit to withhold the masking data for saving a loading time during the testing.

8. The device for fault testing of claim 7, wherein the control unit includes an OR gate.

9. The device for fault testing of claim 1, wherein the masking unit assigns a predetermined value to a failing

latch in the scan string for identifying a location and a test frequency of the failing latch.

10. The device for fault testing of claim 1, wherein the masking unit includes an AND gate.

11. The device for fault testing of claim 1, wherein the loading unit is a multiplexor.

12. A method for fault testing in a microprocessor chip comprising the steps of:

generating a first reference signature which represents faults at a first test frequency;

testing the first reference signature with a target signature;

identifying a failing pattern if the first reference signature is not equal to the target signature;

masking the failing pattern based on masking data and scanning data from a scan string in the chip; and

replacing the first reference signature by a second reference signature which represents a fault at a second test frequency.

13. The method for fault testing in a microprocessor chip of claim 12, wherein the step of masking the failing

pattern further comprises the step of withholding the masking data for saving a loading time during the testing.

14. The method for fault testing in a microprocessor chip of claim 13, wherein the step of masking the failing pattern further comprises the step of shifting bit-by-bit for matching the reference signature with the target signature.

15. The method for fault testing in a microprocessor chip of claim 13, wherein the step of masking the failing pattern further comprises the step of assigning a given value for a failing pattern for identifying a location and a test frequency of the failing pattern.

16. The method for fault testing in a microprocessor chip of claim 12, wherein the step of masking the failing pattern further comprises the step of feeding back the masking data for saving a reloading time after the testing.

17. The method for fault testing in a microprocessor chip of claim 12, wherein the step of masking the failing pattern further comprises the step of exclusively performing the testing to a predetermined latch.